REMARKS

Claim Rejections 35 U.S.C. § 103 (a)

Claims 1-5

The Examiner has rejected claims 1-5 under 35 U.S.C. §103 (a) as being unpatentable over Satya et al. (US 6,528,818) and Browning et al. (US 5,580,829), both previously applied and further in view of Stearns et al. (US 5,715,385).

Applicants respectfully disagree with the Examiner. Applicants have amended claim 1. Support is provided in the specification including in paragraphs [0024], [0025], [0027], [0034], [0036], and [0038] of U.S. 2005/0105792 A1.

Claim 1, as amended, of Applicants' claimed invention, claims a structure (250) disposed near each corner of a die in a space at an intersection of a horizontal scribeline and a vertical scribeline comprising: a first set (245) of features at a particular layer of processing a wafer, said first set of features being a subset of product features, said first set of features surrounded with a number of identical features; and a second set (255) of features adjacent to said first set of features, said second set of features differing from said first set of features in polarity, said polarity referring to placement of an interior of a feature on one side of an edge versus on the other side of the edge. See Figure 3.

In contrast, the Satya et al. reference cited by the Examiner teaches a die array (202), as shown in figure 4A, that includes test dies (204) and product dies (206) separated by scribelines, as shown in Figure 4B, where test structures are located within the test die (204). See Figure 4B. Also, see Col. 11, lines 38-44.

The Examiner states that Satya et al. further teaches that each test die (204) is configured to have a number of portions, namely, a first portion (206) and a second portion (208) separated by an intermediate portion (210). See abstract lines 2-4, 6-8. Also, see col. 37, lines 28-30. Further, see Figure 27, etc.

The Examiner is mistaken in stating that Browning et al. teaches a second set (404) of features that occupies a smaller portion of a space occupied by the structure than a first set (403) of features. See Figure 4 and col. 4, lines 40-52. On the contrary, Browning et al. merely teaches that the first set has larger features (10% oversized), but does **not** teach that the features occupy a larger portion of a space occupied by the structure in a scribeline.

In the opinion of the Examiner, Stearns et al. teaches performing the operations of scaling, translation, or rotation on an entire image or on any part thereof. See col. 1, lines 30-37.

Thus, a combination of the structures of Satya et al., Browning et al., and Stearns et al. would still not produce the structure claimed by Applicants in claim 1, as amended, of Applicants' claimed invention.

Consequently, the three references cited by the Examiner do not, individually or collectively, teach, suggest, or render obvious the structure of Applicants' claimed invention, as claimed in claim 1, as amended, to one of ordinary skill in the art of fabricating semiconductors at the time that the invention was made.

Claims 2-5 are dependent on claim 1, as amended. As discussed previously, Applicants' claimed invention, as claimed in claim 1, as amended, would not have been obvious to one of ordinary skill in the art of fabricating semiconductors at the time that the invention was made. Thus, Applicants' claimed invention, as claimed in claims 2-5, would also not have been obvious to one of ordinary skill in the art of semiconductors at the time that the invention was made.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections to claims 1-5 under 35 U.S.C. §103 (a).

Claims 6-11

The Examiner has rejected claims 6-11 under 35 U.S.C. §103 (a) as being unpatentable over Satya et al. (US 6,528,818), Browning et al. (US 5,580,829) and in view of Stearns et al. (US 5,715,385) as applied to claims 1-5 above and further in view of Gallarda et al. (US 6,539,106).

Applicants respectfully disagree with the Examiner. Claims 6-11 are dependent on claim 1. Support is provided in the specification including in paragraphs [0024], [0025], [0027], [0034], [0036], and [0038] of U.S. 2005/0105792 A1.

Claim 1, as amended, of Applicants' claimed invention, claims a structure (250) disposed near each corner of a die in a space at an intersection of a horizontal scribeline and a vertical scribeline comprising: a first set (245) of features at a particular layer of processing a wafer, said first set of features being a subset of product features, said first set of features surrounded with a number of identical features; and a second set (255) of features adjacent to said first set of features, said second set of features differing from said first set of features in polarity, said polarity referring to placement of an interior of a feature on one side of an edge versus on the other side of the edge. See Figure 3.

In contrast, the Satya et al. reference cited by the Examiner teaches a die array (202), as shown in figure 4A, that includes test dies (204) and product dies (206) separated by scribelines, as shown in Figure 4B, where test structures are located within the test die (204). See Figure 4B. Also, see Col. 11, lines 38-44.

The Examiner states that Satya et al. further teaches that each test die (204) is configured to have a number of portions, namely, a first portion (206) and a second portion (208) separated by an intermediate portion (210). See abstract lines 2-4, 6-8. Also, see col. 37, lines 28-30. Further, see Figure 27, etc.

The Examiner is mistaken in stating that Browning et al. teaches a second set (404) of features that occupies a smaller portion of a space occupied by the structure than a first set (403) of features. See Figure 4 and col. 4, lines 40-52. On the contrary, Browning et al. merely teaches that the first set has larger features (10% oversized), but does **not** teach that the features occupy a larger portion of a space occupied by the structure in a scribeline.

In the opinion of the Examiner, Stearns et al. teaches performing the operations of scaling, translation, or rotation on an entire image or on any part thereof. See col. 1, lines 30-37.

In the opinion of the Examiner, Gallarda et al. teaches both a reference image of contact holes and a test image of contact holes. See col. 6, lines 36-48. However, the reference image is taken at a location on a die while the test image is taken at the **same** location on a **different** die.

Thus, a combination of the structures of Satya et al., Browning et al., Stearns et al., Gallarda et al. would still not produce the structure claimed by Applicants in claim 1, as amended, of Applicants' claimed invention.

Consequently, the four references cited by the Examiner do not, individually or collectively, teach, suggest, or render obvious the structure of Applicants' claimed invention, as claimed in claim 1, as amended, to one of ordinary skill in the art of fabricating semiconductors at the time that the invention was made.

Claims 6-11 are dependent on claim 1, as amended. Thus, Applicants' claimed invention, as claimed in claims 6-11, would also not have been obvious to one of ordinary skill in the art of semiconductors at the time that the invention was made.

Conclusion

Applicants believe that all claims pending, including claims 1-11, of Applicants' claimed invention are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

Pursuant to 37 C.F.R. 1.136 (a) (3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charge or fee, including a Request for Continued Examination, an extension of time fee, or other fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 50-0221.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 653-7897.

Respectfully submitted,

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/George Chen/

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